A 4.9 mΩ-Sensitivity Mobile Electrical Impedance Tomography IC for Early Breast-Cancer Detection System

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***Abstract*—A mobile electrical impedance tomography (EIT) IC is proposed for early breast cancer detection personally at home. To assemble the entire system into a simple brassiere shape, EIT IC is integrated via a multi-layered fabric circuit board which includes 90 EIT electrodes and two reference electrodes for current stimulation and voltage sensing. The IC supports three operating modes; gain scanning, contact impedance monitoring, and EIT modes for the clear EIT image. A differential sinusoidal current stimulator (DSCS) is proposed for injection of low-distortion programmable current which has harmonics less than −59 dBc at a load impedance of 2 kΩ. To get high sensitivity, a 6-channel voltage sensing amplifier can adaptively control the gain up to a maximum of 60 dB, and has low input referred noise, 36 nV/$\sqrt{}$Hz. The 2.5 × 5 mm chip is fabricated in a 0.18 μm 1P6M CMOS process and consumes 53.4 mW on average. As a result, a sensitivity of 4.9 mΩ is achieved which enables the detection of a 5 mm cancer mass within an agar test phantom.**

***Index Terms*—Electrical impedance tomography (EIT), breast cancer detection, mobile healthcare, planar-fashionable circuit board (P-FCB), contact impedance sensing.**

I. Introduction

BREAST cancer is the second cause of mortality after lung cancer. Also, except for skin cancers, breast cancer is the most commonly diagnosed. In 2013, 232,340 new cases of breast cancer were diagnosed in women in the U.S., and about 39,620 women in the U.S. are expected to die from breast cancer [1]. According to World Health Organization (WHO), if breast cancer can be detected and treated in its early stage, one-third of these patients will be cured, and in a world context, this means 400,000 lives could be saved every year. For the early detection of breast cancer, X-ray mammography and ultrasonic screening are the main methods used in hospitals. However, for personal cancer detection at home, only palpation can be used, but this is unscientific and even trained clinicians can misdiagnose using this method. So far, there is no convenient and scientific method which can be used personally by a woman at home for early breast cancer detection.

Electrical Impedance Tomography (EIT) is an imaging technique which calculates the electrical conductivity distribution within the interior of a body from the impedance measurements on its surface [2]. Since malignant breast tissue has about 3 times higher impedance than normal breast tissue and has different impedance characteristics [3], [4], EIT has been studied actively as an alternative breast cancer detection method, and several EIT systems have been developed for breast cancer detection [5]–[7]. The system introduced in [5] is a bed type in which a cone-shaped bucket is formed and filled with liquid electrolyte. An electrode array is constructed on the side of the bucket, and the breast would be dipped into the bucket to contact with the electrodes via the liquid electrolyte. In these systems, the current is dispersed within the liquid before entering into the breast, which results in a low image resolution. Another approach is the probe type system [6], [7]. This system uses an array of metallic rods on the bottom of a probe plate, and a skilled practitioner should press the breast against this plate to measure the tissue impedance profile. In this system, the effective number of electrodes is proportional to the pressure, and only a 2D slice image can be obtained. Therefore, these previous systems have unstable electrode contacts, bulky electronics, and difficult usage which can be handled only by a skilled practitioner. Therefore, they cannot be used personally at home to conveniently detect early stage cancer.

In this paper, a high-resolution EIT IC is proposed to enable a compact, convenient, brassiere-shaped early breast cancer detection system [8]. The integrated system has a small form factor for personal use at home without expertise. The EIT IC employs a low distortion sinusoidal current stimulator and six channels of high sensitivity analog front-end. The EIT IC is integrated on a fabric which has multiple soft electrodes, and these electrodes make secure contact on the contoured surface of the breast. Moreover, the breast EIT image can be reconstructed and displayed on a portable smart device so that the user can get images easily at home.

The rest of the paper is organized as follows. In Section II, the proposed early breast cancer detection system will be explained. Section III discusses the detailed implementation of the EIT IC

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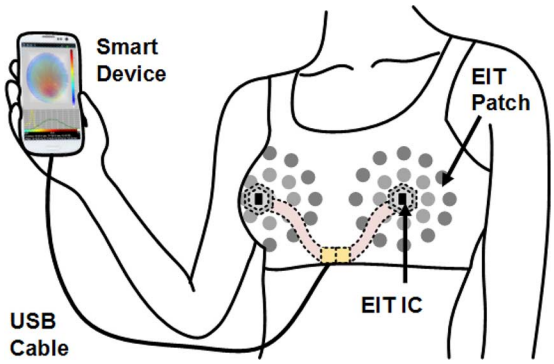


Fig. 1. The proposed personal early breast cancer detection system.

including 1) reconfigurable measurement modes, 2) Differential Sinusoidal Current Stimulator (DSCS), 3) 6-channel analog front-end, and 4) digital controller. Section IV shows the implementation and measurement results, and finally Section V concludes the paper.

II. System Overview

The overall system architecture of the proposed early breast cancer detection system is shown in Fig. 1. It is composed of three functional components: electrode array, electronic circuitry, and imaging device. In the previous bed type and probe type systems, the electrode contact is unstable because the electrode array is made of rigid metal. Also, the electronic circuitry is contained in a big box, and a large computer is used as the imaging device. Therefore, the previous systems are not portable and cannot be used personally. In this proposed system, the electrode array is patterned on fabric using Planar-Fashionable Circuit Board (P-FCB) technology [9]–[11] to make the soft electrodes contact securely on the breast. The full electronic functionality is implemented by a customized EIT IC to make the system small and compact. In addition, a portable smart device which can be connected via the USB port is conveniently used for imaging and displaying.

Fig. 2 shows the structure of proposed EIT patch fabricated using P-FCB technology. The hemispherical EIT patch (12 cm diameter and 5 cm height) has three layers: 1) the electrode array layer; 2) the electrode connection layer; and 3) the electronic circuit layer. To measure EIT with sufficient sensitivity to enable breast cancer cell detection down to ~ 5 mm with this patch, the detectable and reconstructible volume ratio according to the number of electrodes is simulated as shown in Fig. 3(a). The electrode size was varied and stimulation current was set to 100 $\mu A_{p\text{-}p}$ which is the maximum amplitude at 100 Hz allowed, to comply with the relevant medical standards IEC60601-1 [15]. The simulation results shows that the number of electrodes should be greater than 80 to detect and reconstruct a cancer model which has volume of $\sim 0.1\%$ of breast model. Therefore, 90 EIT electrodes and 1 voltage reference electrode each of diameter 8 mm are implemented on the electrode array layer. For the prototype system, the 90 EIT electrodes are arranged as 5 concentric circles, and each circle has 6, 12, 18, 24, and 30 electrodes respectively so that all distances between neighboring electrodes are equal. The electrode array and EIT IC is connected via an electrode connection layer, and EIT IC is wire-bonded and molded on the topmost electronic circuit layer. All three layers are implemented by P-FCB process and stacked [12], [13] to form the brassiere shape. The EIT patch is covered by a cloth stuffed with pads to push the electrodes on to the breast skin to make a secure electrical contact. At the end of the communication line, a current reference electrode and USB cable connector are placed at the lower edge of the joint of two EIT patches.

Ag/AgCl paste, not the gel type, is deposited to form dry electrodes on the fabric. These P-FCB electrodes are flexible like silk cloth so that they can follow the contours of the breast smoothly to achieve a secure electrical contact. Since the P-FCB electrode is dry, users would not suffer from the irritation which can occur with gel type Ag/AgCl. As shown in Fig. 3(b), the electrode-skin contact impedance of P-FCB electrodes using Ag/AgCl paste is typically 2 kΩ at 1 kHz. 100 Hz–100 kHz signals are usually used in the EIT system, and these measurements show that the contact impedance of dry P-FCB electrode is higher than wet type Ag/AgCl electrode at low frequency. Therefore, the proposed system is specially designed to take this high contact impedance into consideration, and this will be discussed in Section III.

III. Electrical Impedance Tomography (EIT) IC

Fig. 4 shows the overall block diagram of the proposed electrical impedance tomography (EIT) IC architecture. It consists of four functional blocks: 1) a switching network for reconfigurable measurement modes; 2) Differential Sinusoidal Current Stimulator (DSCS) to inject the programmable single-tone current signal; 3) 6 channel analog front-end to measure voltages with high sensitivity and perform digitization; 4) digital controller for system control and data calibration.

Several imaging methods have been reported so far, and among them the differential method is generally used to get the clear EIT image. The differential method takes an initial measurement result as the reference data and later measurements results are compared with the reference data to obtain the impedance difference for the imaging. There are two types of differential imaging methods; the time difference and the frequency difference methods. For the imaging of the time varying organs, such as respiration or cardiac cycle, the time difference method is used, and the several measurements according to the time are needed to obtain the EIT images via temporal impedance variation. However, since breast cancer tissue is static, there is no temporal impedance difference between the measurements. Therefore, the frequency difference method [14] should be used. Since the impedance change versus frequency in healthy breast tissue is different to that in malignant tissue [3], [4], measurements at two different frequencies are used to obtain a static EIT image. A current stimulator is designed to inject current signals at 100 Hz, 1 kHz, 10 kHz, 100 kHz, because the largest impedance variations are measured in the range from 1 kHz to tens of kHz. Therefore, the measurement data at low frequency (below 1 kHz) is used

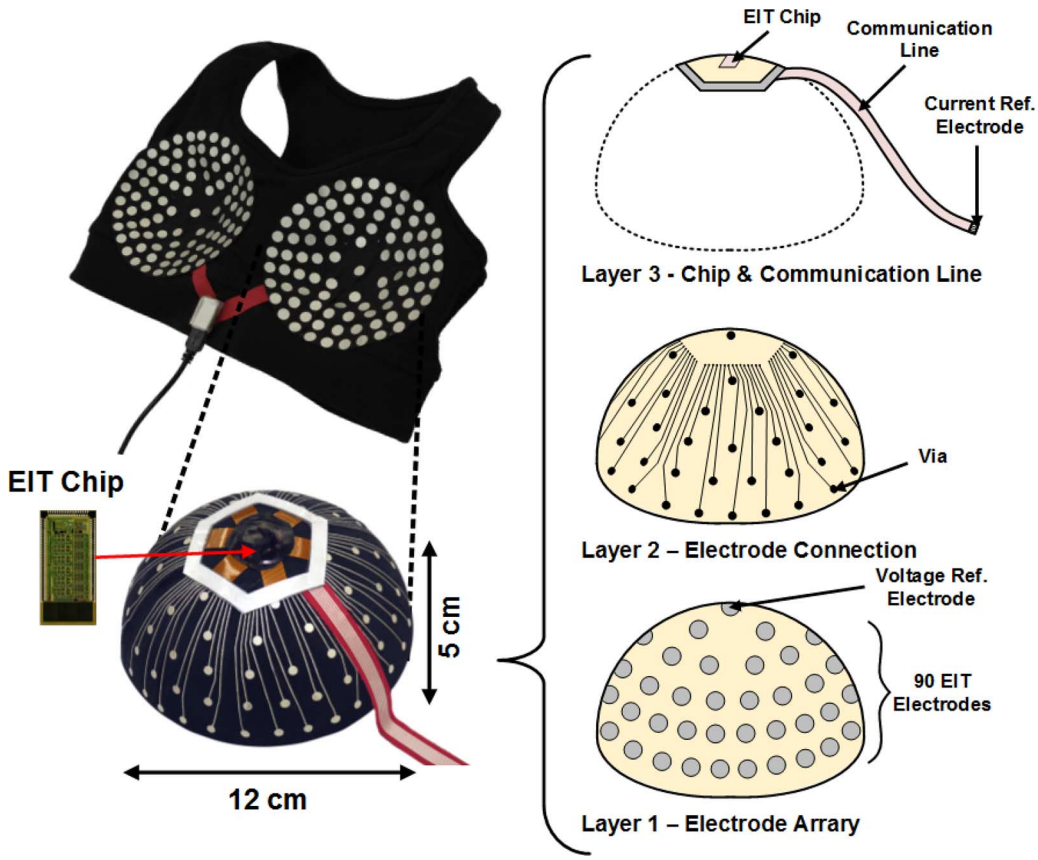


Fig. 2. The proposed electrical impedance tomography (EIT) patch.

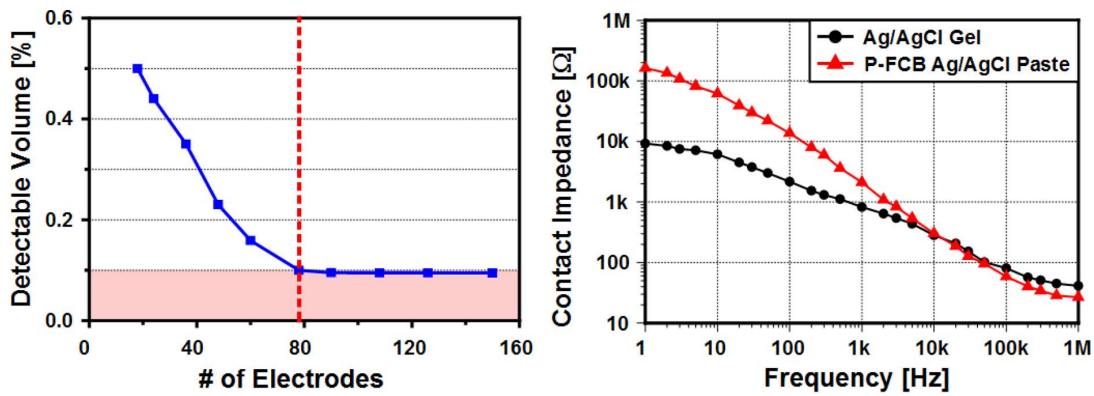


Fig. 3. (a) Detectable size of breast cancer cell. (b) Electrode-skin contact impedance of P-FCB electrode.

as the reference. Also, the current amplitude of 10–400 $\mu A_{p\text{-}p}$ which is varied according to the frequency, is used to satisfy the safety regulations for medical electrical equipment [15]. The DSCS is designed with high output impedance (larger than 100 kΩ) to prevent the mismatch and the load impedance variation of the current stimulator.

Fig. 5 shows a simulation using 30 electrodes, whereby adjacent electrode pairs are stimulated with 400 $\mu A_{p\text{-}p}$ current and the resulting voltages are measured. The simulated voltage amplitudes at the adjacent pairs of electrodes are in the range of 0.27–17.7 mV according to the position of the electrode pair. The output voltage has a wide dynamic range since the maximum voltage is about 65 times of minimum voltage, while the minimum voltage variation is only a few μV. Therefore, to detect such a small variation over a wide dynamic range, the analog front-end should have high sensitivity, and also be able to control its voltage gain automatically according to the electrode position. Moreover, a current stimulator with low distortion, and a low noise ($<1\,\mu V/\sqrt{Hz}$) voltage amplifier are required to get sufficiently high SNR voltage signals. Any harmonic distortion in the applied current signal can cause measurement errors, especially during signal demodulation. In this system, we use a peak-to-peak detector (PPD) to demodulate the measured signal, thus the spectral purity of the stimulation signal is particularly important.

With 90 electrodes, up to $90 \times 89 = 8010$ voltage measurements are required. For less than 1 minute scanning time at the lowest frequency (100 Hz), the number of voltage sensing

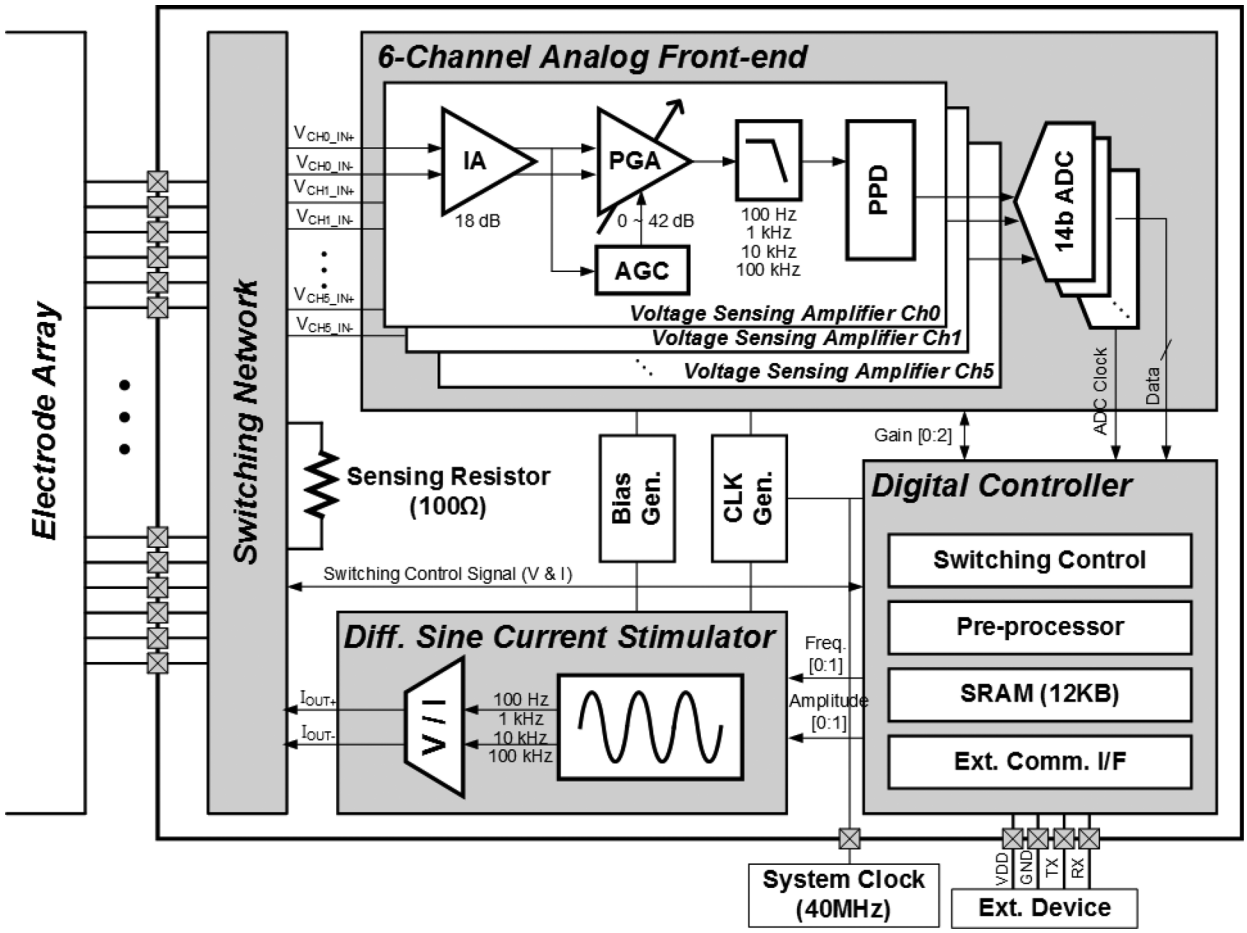


Fig. 4. Overall block diagram of electrical impedance tomography IC.

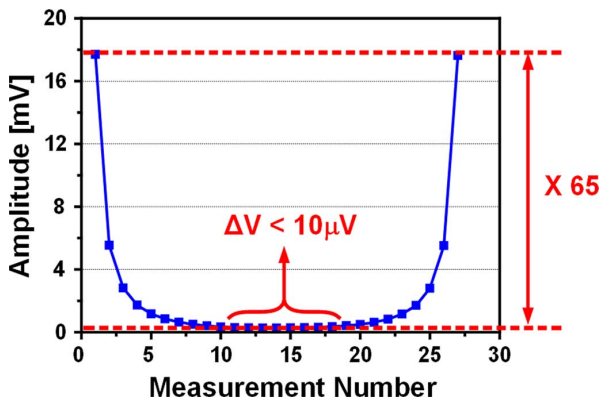


Fig. 5. Input voltage amplitude of EIT measurement.

channels should be greater than 5. Moreover, in this proposed system, 90 electrodes are arranged as 5 concentric circles, and the numbers of electrodes in each circle is a multiple of 6. Therefore, the number of voltage measurement channels is determined as 6.

A. Reconfigurable Measurement Modes

The proposed system has three operating modes depending on the configuration of the switching network. The first is a gain scanning (GS) mode to obtain gain mismatch information of the six voltage measurement channels, because the channel mismatch can determine the overall measurement error [23]. Fig. 6(a) shows that in GS mode, the current stimulator and each of the voltage sensing amplifiers in the analog front-ends are connected via an internal 100 Ω sensing resistor through the switching network with the current stimulator set to 10 $\mu A_{p\text{-}p}$. The digital controller samples the measured voltage of each channel and calculates the channel gain mismatch information which is stored and used to calibrate each channel during EIT operation.

The second mode involves contact impedance monitoring (CIM), to check whether the electrodes are in reliable contact with the breast skin or not. A low and stable contact impedance is very important to maximize system accuracy. Since the contact impedance is a major portion of the load impedance of the DSCS, it determines the maximum allowable amplitude of the stimulation current. In CIM mode, the analog front-end measures the voltage developed on a pair of electrodes while the current source injects 10 $\mu A_{p\text{-}p}$ to the same pair of electrodes, and this step is repeated for all 90 electrodes. Then, the digital controller calculates the contact impedance of each electrode and divides the electrodes into four groups according to their contact impedance values (Good, Average, Bad, No Contact). The quality of contact, or the range of the contact impedances, can be depicted as shown in Fig. 6(b), and this information can

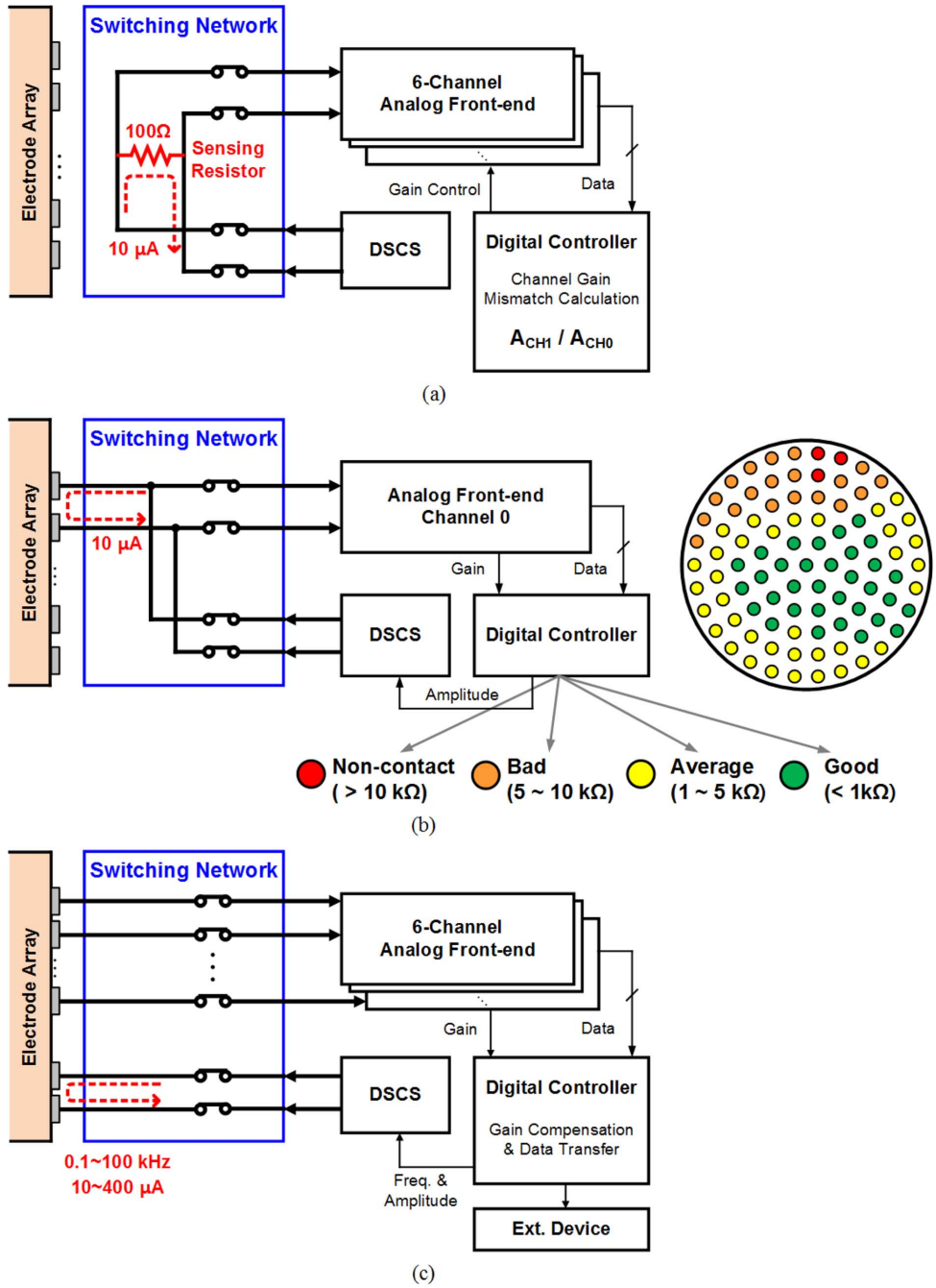


Fig. 6. Reconfigurable measurement modes. (a) Gain scanning mode. (b) Contact impedance monitoring mode. (c) EIT mode.

be used for manual calibration (position adjustment) to ensure an initial stable contact. Moreover, the contact impedance information is stored in the digital controller and used not only to determine the amplitude of stimulation current, but also subsequently to calibrate the image.

In EIT mode, the current is injected between two electrodes, while six channels of analog front-ends are connected to the different pairs of electrodes in turn until the voltages of all electrode pairs are measured (Fig. 6(c)). The digital controller combines all the data and gain mismatch information obtained in other modes and compensates for the channel gain mismatch to reduce its variation to less than 0.2 mV among channels. Then, the digital controller transmits the calibrated data to the external imaging device. The pairs of electrodes in the EIT mode are freely selected by programming the switching network to support various imaging algorithms. For example, the pairs of electrodes can be sequentially selected in the EIT electrodes as shown in Fig. 7. Or in another algorithm, the current signal can be injected between one EIT electrode and the current reference electrode, and the voltages measured between another EIT electrode and the voltage reference electrode.

B. Differential Sinusoidal Current Stimulator (DSCS)

The generation of a single-tone sinusoidal current is one of the most power consuming sections, and also the most difficult

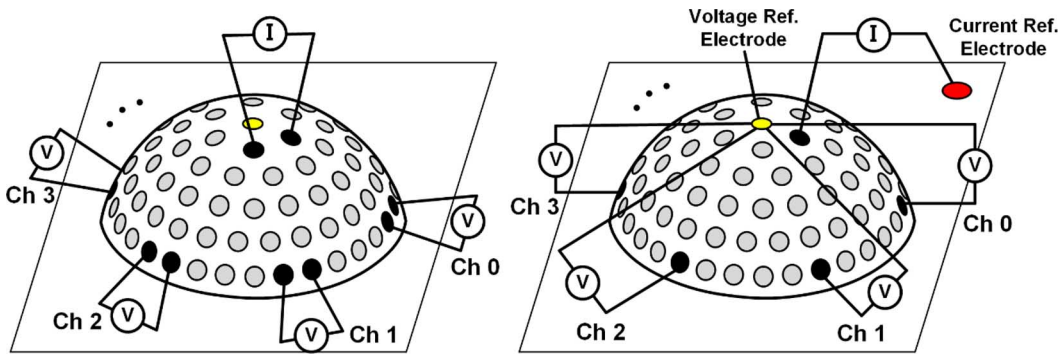


Fig. 7. Selection of EIT electrode pair.

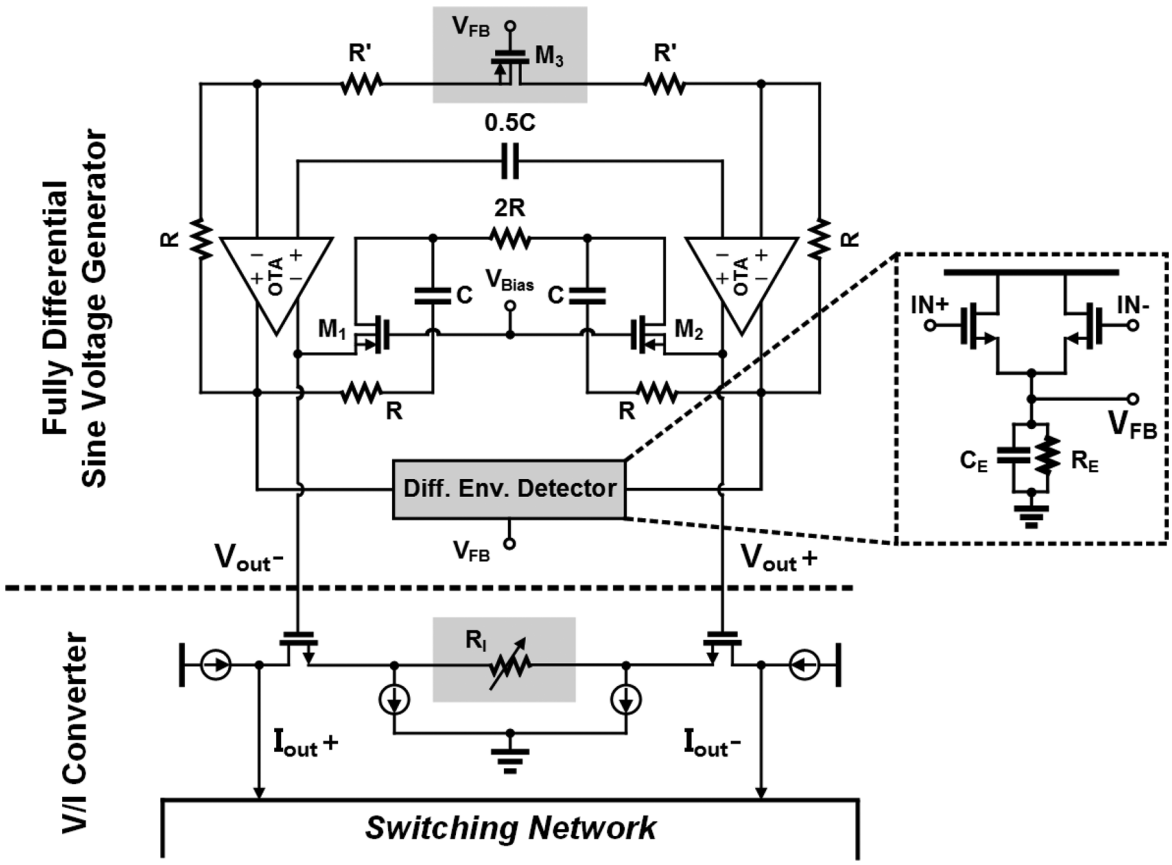


Fig. 8. DSCS circuit.

to implement. Most previous EIT systems implemented the current stimulators by using FPGA-based direct digital synthesizer (DDS) [16], [17], but these current stimulators were bulky and showed low accuracy. On-chip DDS is possible [22], but requires a high-speed DAC and sharp BPF to reduce harmonic distortion, and typically consumes a lot of power. Fig. 8 shows the proposed DSCS circuit composed of two fully differential amplifiers and an RC bridge network with careful layout for balanced voltage generation [18]. The resistors and capacitors in the RC bridge network are scaled to generate four different frequencies (100 Hz, 1 kHz, 10 kHz, 100 kHz). $\mathrm{R} = 80\ \mathrm{k}\Omega$ and $\mathrm{C} = 18$ pF is used to generate a 100 kHz sinusoid. The second-order harmonic is greatly reduced by the differential signaling, but the third-order harmonic remains at -42 dBc. Therefore, in this DSCS, an envelope detector is added to continuously adjust the loop gain. The differential envelop detector with on-chip resistor ($\mathrm{R_E} = 8\ \mathrm{M}\Omega$) and small off-chip capacitor ($\mathrm{C_E} = 1.8$ nF, SMD 1608) senses the amplitude of the output voltage, $\mathrm{V_{FB}}$, and feeds it back to the gate of M3 so that the resistance in the RC network can be controlled. As a result, the output voltage swing is stabilized by adjusting the loop gain, and the third-order harmonic can be reduced to -65 dBc.

Through a V/I converter, the output voltage of the differential sinusoidal voltage generator $(\mathrm{V_{out+}} - \mathrm{V_{out-}})$ is converted into a differential sinusoidal current $(\mathrm{V_{out+}} - \mathrm{V_{out-}})/\mathrm{R_I}$. The amplitude of the output current can be controlled by changing the value of $\mathrm{R_I}$ via a 2 bit digital code to inject 10, 100, 200, or 400 $\mu\mathrm{A_{p\text{-}p}}$ of current to the selected electrodes.

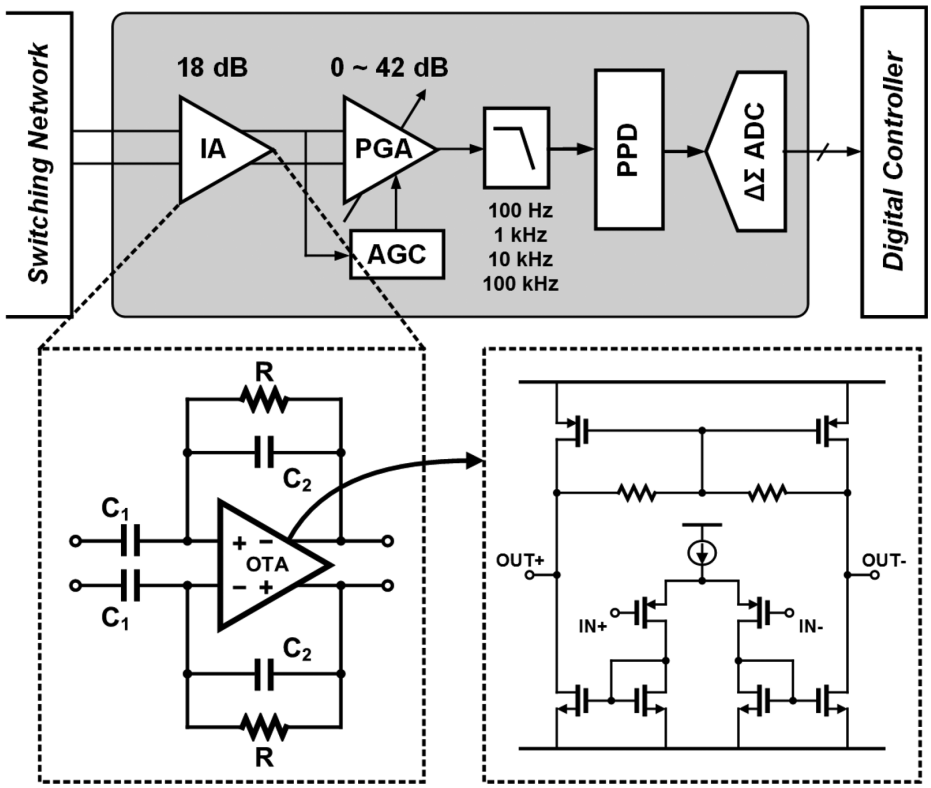


Fig. 9. Analog front-end circuit.

C. Six-Channel Analog Front-End

Fig. 9 shows the analog front-end circuit. Each analog front-end channel comprises an instrumentation amplifier (IA) as the LNA, a programmable gain amplifier (PGA), an adaptive gain controller (AGC) to support large dynamic range, a low-pass filter, a peak-to-peak detector (PPD) as a demodulator, and a $\Delta\Sigma$ ADC.

The IA is a fully differential capacitive-coupled IA [19]. This IA has low noise, high input impedance, and well-defined voltage gain set by the ratio of the input capacitor, $\mathrm{C1}$, and the feedback capacitor, C_2. Moreover, the HPF cut-off frequency can be set by R and C_2, so that rail-to-rail electrode DC offset cancellation can be realized. This HPF in IA can avoid signal saturation due to DC offsets and thus maximize the input dynamic range. In this design, because the expected maximum voltage value (Fig. 5) is ~ 18 mV, the gain of IA is set to 18 dB to prevent signal saturation. The IA exhibits input referred noise of 36 nV/$\sqrt{}$Hz, and a common mode rejection ratio (CMRR) over 90 dB.

The PGA of the same architecture as IA has two stages with AGC to amplify the large input voltage variation as shown in Fig. 10. In the first AGC stage, the PGA inputs are compared with a pre-determined reference voltage $\mathrm{V}_{\mathrm{ref0}}$ (950 mV). A dynamic comparator is used, and the clock frequency is chosen 50 times faster than input frequency. After switching the electrode pair, the AGC is reset to providing gain of 24 dB, and gain is set to 0 dB until next reset once the amplitude of input exceeds the reference voltage. In the same manner, the second stage of AGC compares the output of the first stage PGA with three reference voltages and provides a 2 bit gain control signal. As a result, the total gain of the PGA can be reconfigured from 0 dB to 42 dB with 6 dB steps automatically according to the gain control signal. When the system operates in GS mode, the AGC is disconnected and the gain of PGA is controlled by the digital controller.

For the EIT measurement, only the amplitude of the sinusoidal signal is needed. Therefore, a PPD is adopted to alleviate the high speed requirement of a complete ADC. As shown in Fig. 11, the input S/H circuit holds the input signal for one clock cycle so that the comparator can detect the highest and lowest peak of the input. The clock frequency for input sampling is chosen about 50 times faster than the input frequency, which is optimized to avoid error due to noises or spikes. To reduce the gain error of the PPD, the clock is synchronized with the input signal so that rising edge of the clock can pick the highest and lowest peak of the input. The gain of the PPD is approximately 0.98 V/V.

The 14 bit $\Delta\Sigma$ ADC is implemented for high resolution, and this can provide hundreds of μV resolution. It is composed of a third-order 1 bit $\Delta\Sigma$ modulator and digital decimation filter. The oversampling ratio of the $\Delta\Sigma$ modulator is 64, and the clock for ADC can be selected from 10 kHz to 40 MHz according to the frequency of stimulation current. The decimation filter is a fourth-order cascaded integrator comb (CIC) filter.

D. Digital Controller

Fig. 12 shows the block diagram and timing diagram of the digital controller. The digital controller is composed of

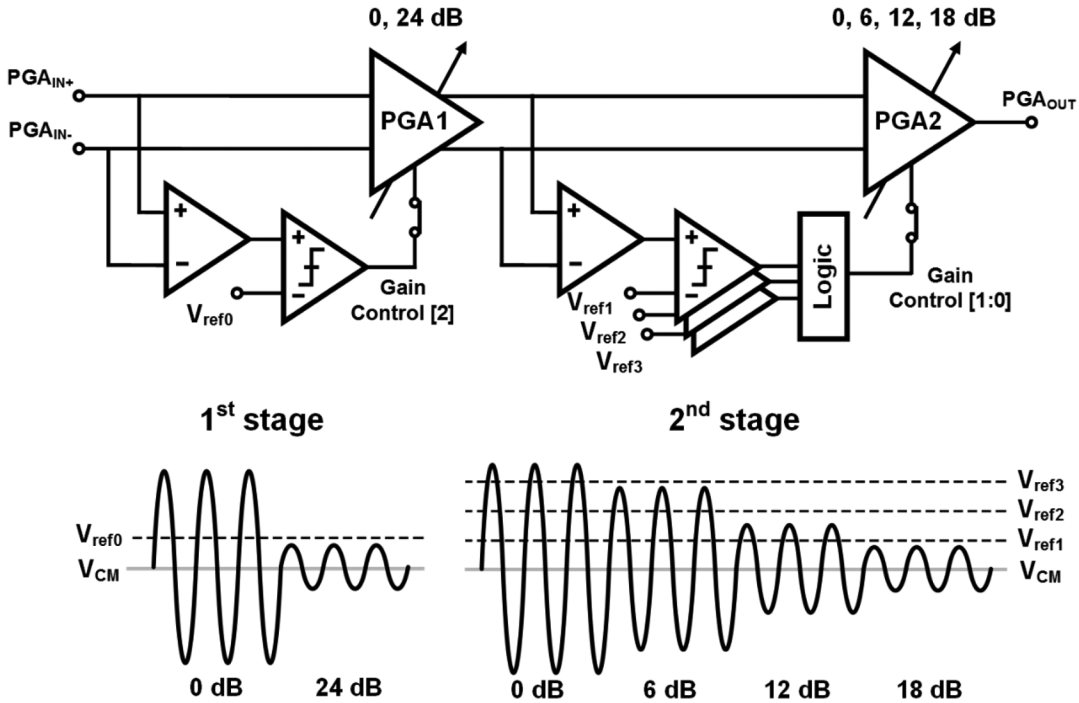


Fig. 10. Two-stage AGC circuit.

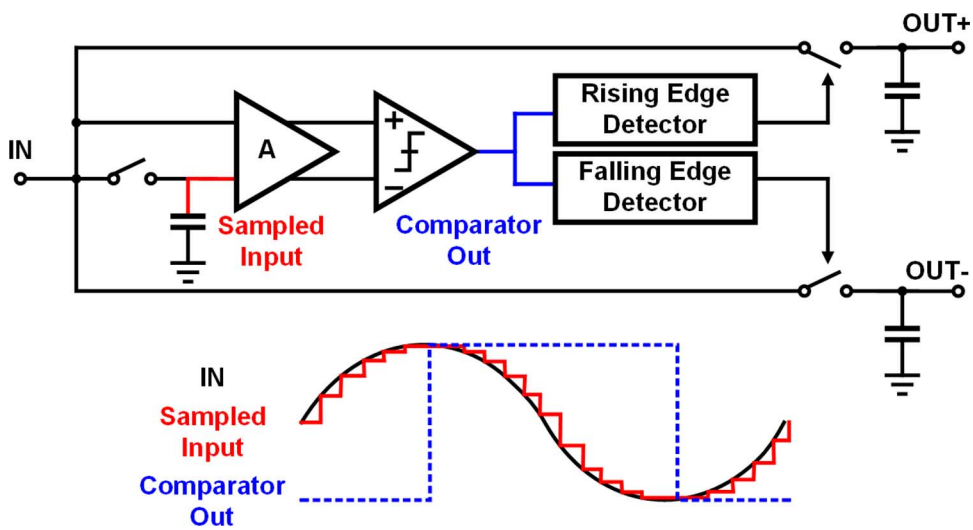


Fig. 11. PPD circuit.

controller, memory, and UART interface. First, the controller accepts the electrode switching sequence from instruction memory (IMEM). Then, it generates the switching signals to reset the analog front-end and to change the electrode configuration in the switching network. During one electrode connection, the ADC samples the demodulated voltage signal N times according to the preset frequency of the ADC clock. Therefore, after N data words are collected, the controller calculates the average which is then stored in data memory (DMEM) together with the gain control codes generated by the AGC.

When the electrode switching sequence is complete, the stored data is used to calibrate for channel gain mismatch reduction. In GS mode, the gain of each channel is measured individually and then all six channel gains are averaged to obtain the reference channel gain. The gain deviation of each channel from the reference gain is stored in memory, and later the stored gain deviation is added to or subtracted from the measured data at each channel. Finally, the calibrated data is transmitted to the external smart device through the UART interface.

IV. Implementation and Measurement Results

A. Electrical Impedance Tomography IC Implementation Results

Fig. 13(a) shows the output spectrum of the DSCS while providing 200 $\mu A_{p\text{-}p}$ of sinusoidal current with a load resistor

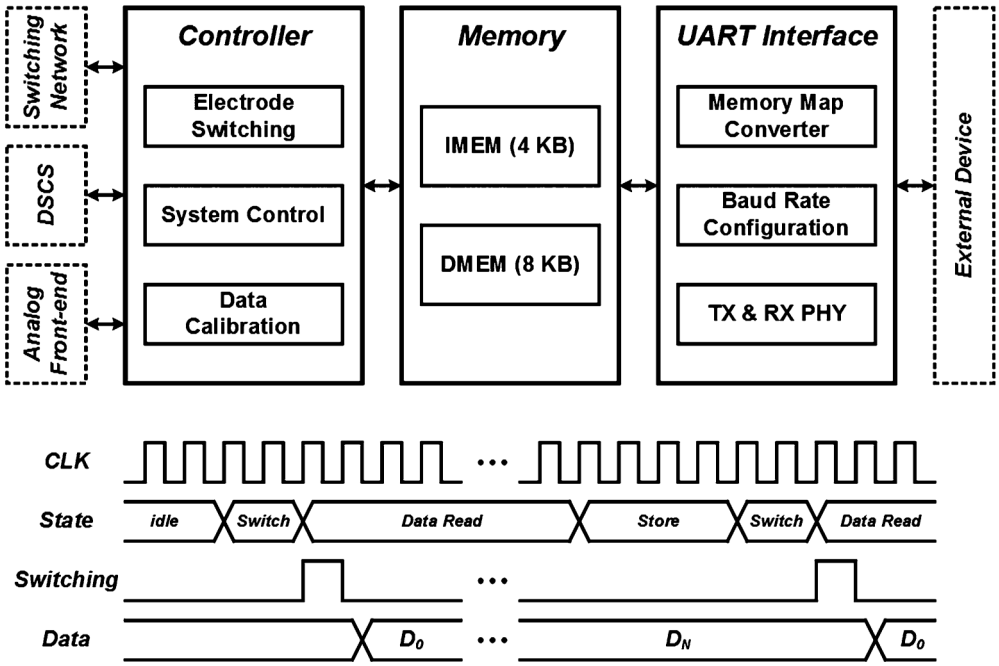


Fig. 12. Block diagram and timing diagram of the digital controller.

of 2 kΩ. Differential sinusoidal currents of 122 Hz, 1.23 kHz, 12.8 kHz, and 121.7 kHz are generated, and these 4 frequencies can be selected via a 2 bit digital code. All harmonics are less than −59 dBc, and especially the third-order harmonic of the DSCS is reduced by 43% compared with our previous work [18]. As shown in Fig. 13(b), the amplitude of the current can be increased from 10 $\mu A_{p\text{-}p}$ to 400 $\mu A_{p\text{-}p}$ by controlling the resistor in the V/I converter with 2 bit digital control signal, and the current amplitude is decided according to the measured contact impedance in CIM mode. Therefore, 400 $\mu A_{p\text{-}p}$ of current can be provided up to 1 kΩ of load impedance with maximum current variation of 1%, and this amplitude is selected when all electrodes are in good contact (<500 Ω of contact impedance).

AGC measurements as the input signal is decreased 14 mV to 2 mV are shown in Fig. 14(a). When the AGC is turned off and the total gain of amplifier is set to 18 dB, the output signal of PGA also decreases, following to the input. However, when the AGC is turned on, the 3 bit gain control signal of PGA is adaptively changed. Fig. 14(b) shows the measured output of ADC when the AGC is activated or not. With the help of AGC, all input signals from a few μV to tens of mV can be adaptively amplified into mV-scale. The measurement results of PPD are shown in Fig. 15. As the peak detection pulse is set to high at the highest or the lowest peak of the input signal, the differential output of PPD represents the amplitude of the input sinusoidal signal. Fig. 16 shows the electrode switching signal from the digital controller. In EIT mode, when the electrode switching signal is high, the electrode configuration changes to the next configuration by the digital controller, and the output PGA is changed according to the selected electrode pair.

The proposed EIT IC is fabricated in 0.18 μm 1P6M CMOS technology, and occupies 2.5 mm×5 mm chip area including pads as shown in Fig. 17. Table I summarizes the performance of

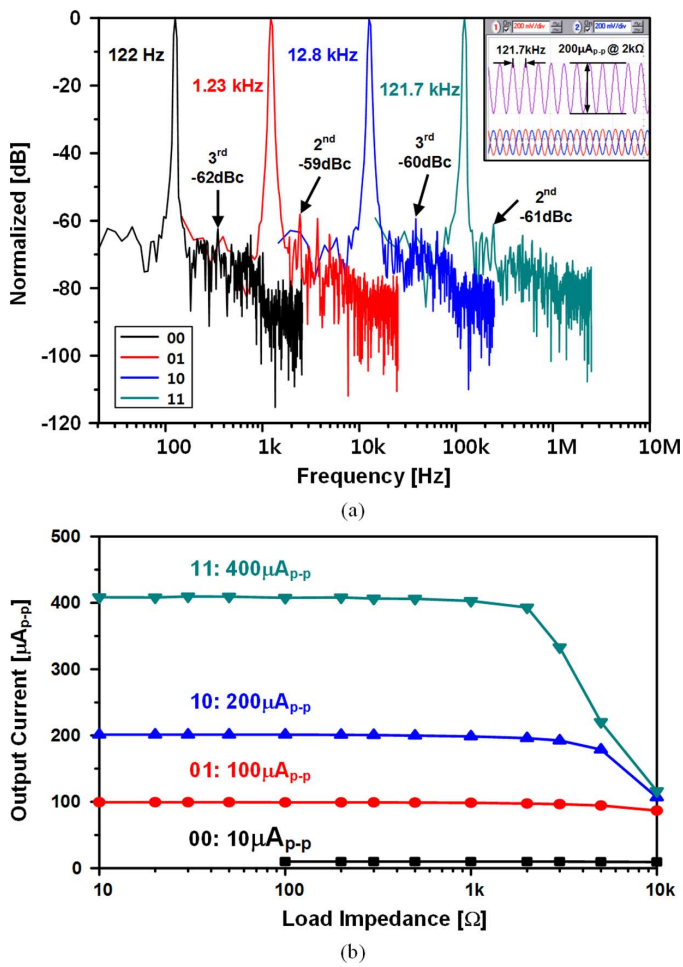


Fig. 13. (a) Output spectrum, and (b) output current stability of DSCS.

the proposed IC. The power is supplied via the USB port, and the average power consumption is 53.4 mW. The proposed DSCS

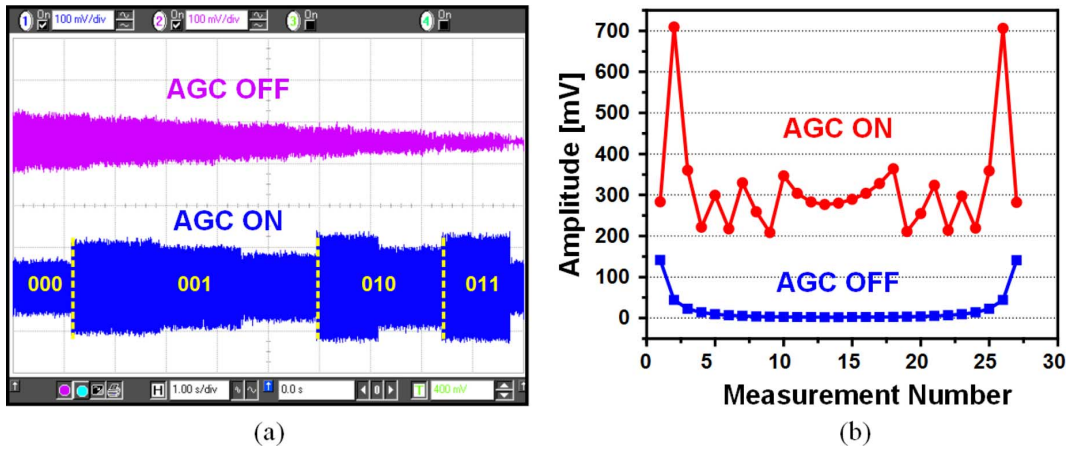


Fig. 14. Measurement result of AGC (a) time domain measurement (b) phantom measurement.

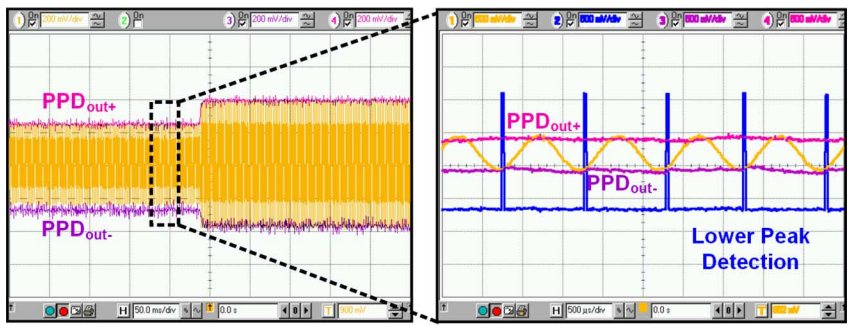


Fig. 15. Measurement result of PPD.

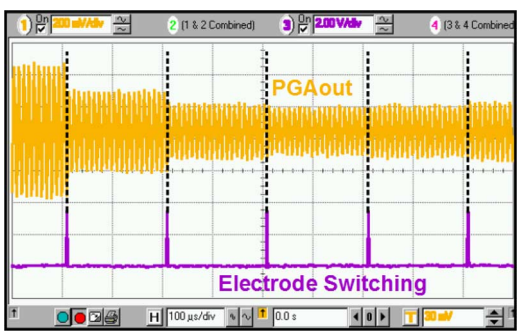


Fig. 16. Measurement result of electrode switching by digital controller.

can stimulate 100 Hz, 1 kHz, 10 kHz, and 100 kHz sinusoidal current with 10 $\mu A_{p\text{-}p}$ to 400 $\mu A_{p\text{-}p}$ of amplitude, and shows less than 0.2% total harmonic distortion (THD). The 6-channel voltage sensing amplifier provides a total voltage gain of 18 dB to 60 dB which is adaptively controlled with 6 dB gain steps. The achieved input referred noise density is 36 nV/$\sqrt{}$Hz, enabling the measurement of impedance differences as small as 4.9 mΩ. The digital controller containing 12 KB on-chip SRAM operates at 40 MHz.

B. Breast Cancer Detection System Measurement Results

Fig. 18 illustrates the measurement set-up for EIT imaging using the proposed breast cancer detection system. The measurement is performed using a breast model made of agar and

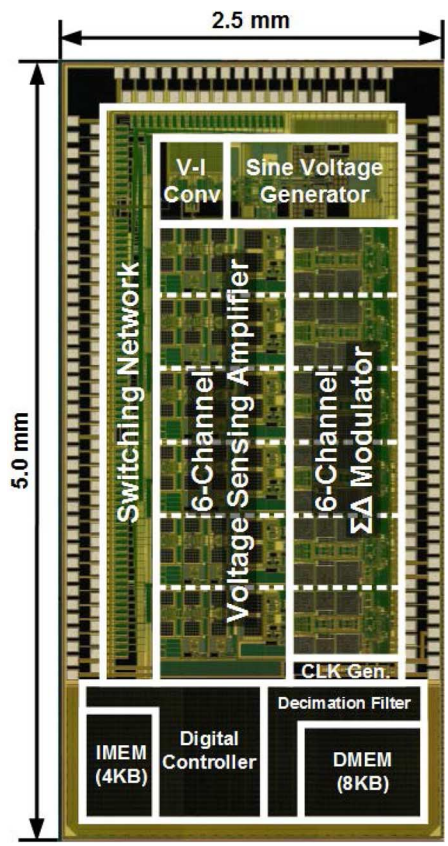


Fig. 17. Chip micrograph.

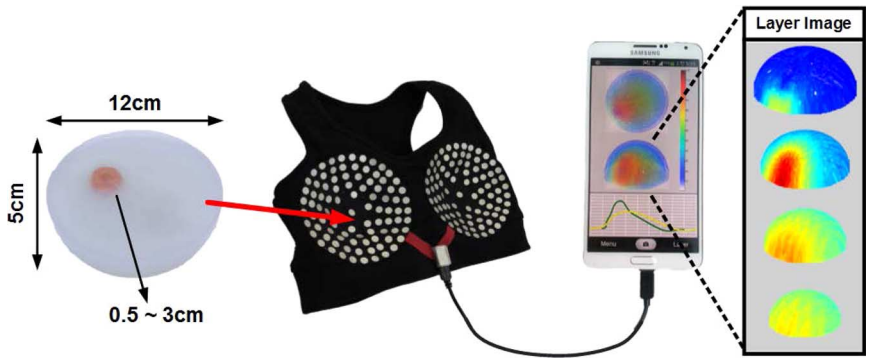


Fig. 18. Measurement set-up of proposed breast cancer detection system.

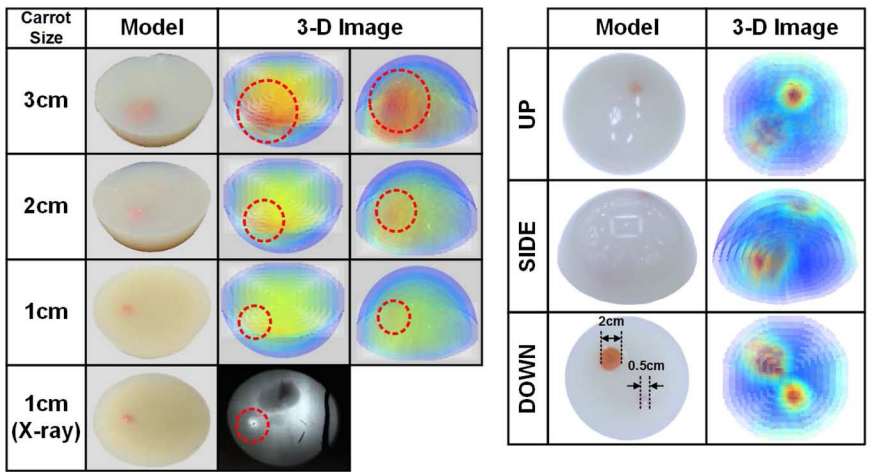


Fig. 19. Breast model imaging results.

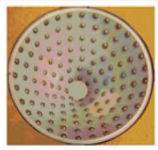
carrot, since agar and carrot have similar impedance characteristics to normal breast tissue and cancer cells, respectively. The 12 cm diameter and 5 cm height of hemispherical agar containing a small carrot 'tumor' is put into the proposed system, and EIT images are displayed on the smart device. The weighted back-projection algorithm [20], which assumes that the electric current is injected through one of the electrodes in a surface array and equipotential surfaces from the electrode are spherical, is used with modification for 3D image reconstruction. The final 3D EIT image can be also displayed as layer images. The reconstructed 3D EIT images with several breast models are shown in Fig. 19. The system with the EIT IC can detect smaller than 1 cm of carrot in the agar, and an x-ray mammography image of the same breast model is also shown for comparison. The proposed system can detect a tumor of 0.1% of breast volume, which is a 5 mm sized carrot in this measurement. Thus, the system has been optimized for the average breast size of Asian women, and a 5 mm size tumor detection corresponds with stage 1 breast cancer. The tumor in stage 1 (smaller than 2 cm) can be completely removed by breast-conserving surgery, and if the tumor is smaller than 1 cm, chemotherapy is not usually offered. The total scanning time of CIM and EIT mode in this system takes typically less than 10 s; during this time the user should stay still to ensure an accurate result.

TABLE I
CHIP PERFORMANCE SUMMARY

Process	**0.18 μm 1P6M CMOS**	
Die Size	**2.50 mm × 5.00 mm**	
Supply Voltage	**1.8 V**	
Power Consumption	**53.4 mW (USB supply)**	
DSCS	**Frequency**	**0.1 ~ 100 kHz (4 step)**
	Amplitude	**10 ~ 400 μA_{p-p}**
	THD	**< 0.2% @ 200 μA_{p-p}**
Analog Front-end	**# of Channels**	**6**
	Gain	**18 ~ 60 dB (6 dB step)**
	Bandwidth	**0.1 ~ 100 kHz**
	Input Noise	**36 nV/√Hz**
	Sensitivity	**4.9 mΩ**
	ADC Clock Freq.	**10 kHz ~ 40 MHz**
Digital Controller	**Operating Freq.**	**40 MHz**
	On-chip SRAM	**DMEM: 8 KB IMEM: 4 KB**

Table II shows the system in comparison to previous EIT systems for breast cancer detection. The proposed system is small and light-weight with flexible electrodes, and 3D imaging can be done using mobile devices. Moreover, it provides contact impedance monitoring and calibration. As a result, the proposed

TABLE II
SYSTEM COMPARISON RESULTS

System	Duke Univ. [5]	Dartmouth [21]	TransScan [7]	MEIK [6]	This Work
System Type					
	Bed	Bed	Probe + Ref. electrode	Hand-held device + Ref. electrode	Brassiere (Wearable)
Dimension	11.7 cm height, 19.1 cm diameter	60 cm diameter (Al annulus)	7.2 x 7.2 cm (electrode)	16 x 18 x 10 cm	30 x 25 x 5 cm
Weight	N/A	N/A	N/A	2 kg	72 g
Image Dimension	2D slices	3D	2D	2D slices	3D
Z_{cont} Monitoring	X	X	X	O	O
Imaging Device	Computer	Computer	Computer	Computer	Mobile Device
Electrodes	128 (7 layers)	64 (4 layers)	256 (planar)	256 (planar)	92 (Flexible)
Frequency	n/a	10 kHz - 10 MHz	58 Hz - 5 kHz	10 kHz, 50 kHz	100 Hz - 100 kHz
Amplitude	1 mA	N/A	1 ~ 2.5 V	0.5 mA	10 μA ~ 400 μA
SNR	77 dB	94 dB	N/A	N/A	90 dB
Minimum Detectable Size	12 mm (in 19.1 cm)	N/A	N/A	N/A	5 mm (in 12 cm)

system can potentially detect breast cancer tumors as small as 5 mm personally at home.

V. CONCLUSION

A compact and convenient early breast cancer detection system is proposed and implemented with a high-sensitivity EIT IC. The proposed EIT IC provides 10 $\mu A_{p\text{-}p}$ to 400 $\mu A_{p\text{-}p}$ of current stimulation and 18 to 60 dB of voltage gain. The DSCS is implemented for low distortion current stimulation, and all harmonics across the stimulation frequency range (0.1–100 kHz) are less than -59 dBc. In the analog front-end, the input referred noise of voltage sensing amplifier is 36 nV/$\sqrt{\text{Hz}}$, and the gain is automatically controlled in 6 dB steps by AGC. The proposed IC occupies 2.5 mm$\times$5 mm including pads in a 0.18 μm 1P6M CMOS technology, and it is incorporated into a 12 cm diameter $\times$5 cm height hemispherical fabric patch. The overall system has a convenient brassiere shape, and can be connected to a mobile smart device to detect breast cancer models as small as 5 mm with 4.9 mΩ sensitivity. As a result, the proposed system with fully integrated EIT IC potentially enables early breast cancer detection at home.

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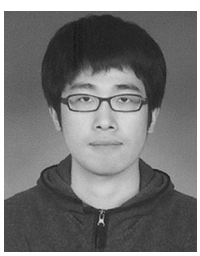

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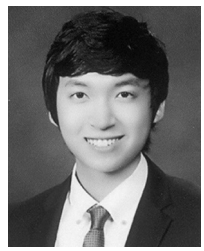

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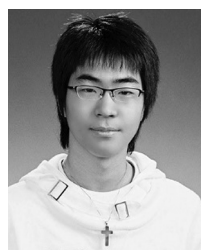

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